Ananda Samajdar

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Research Interests

Compilation for custom architectures, Deep learning accelerators, Machine learning Computer architecture, Architecture for continuous learning, VLSI design

Education

- **Georgia Institute of Technology** — **Atlanta, GA**
  PhD, Electrical and Computer Engineering — *2016–2021*
  Advisor: Prof. Tushar Krishna
- **Indian Institute of Information Technology** — **Allahabad, India**
  B.Tech. (Hons), Electronics and Communication Engineering — *2009–2013*

Professional Experience

- **IBM Research, TJ Watson Research Center** — **Yorktown Heights, NY**
  Research Scientist — *Feb 2022–Present*
  - Hardware Software co-design for AI workloads
- **Georgia Institute of Technology** — **Atlanta, GA**
  Graduate Research Assistant — *Jan 2017–Dec2021*
  - Pursuing graduate research at Synergy Lab
- **Microsoft, Azure HSG** — **Redmond, WA**
  AI and Research Intern — *May 2019–Aug 2019*
  - Exploring architectural optimizations for Azure workloads
- **ARM Research** — **Boston, MA**
  Machine Learning Research Intern — *May 2017–Nov 2017*
  - Developed SCALE-Sim, a simulator for systolic-array based CNN accelerators
  - Algorithm-Hardware co-design for energy efficient mobile continuous vision
- **Qualcomm India Pvt Ltd** — **Bangalore, India**
  Engineer, SoC Design-Power — *Dec 2015–Jun 2016*
  - RTL designer for power management subsystem for Snapdragon SoCs
  - Power intent designer for SoC top level
- **Qualcomm India Pvt Ltd** — **Bangalore, India**
  Associate Engineer, SoC Design-Integration — *Aug 2013–Nov 2015*
  - RTL designer for top level Snapdragon SoC subsystems
  - SoC connectivity, integration and debug designer

- **Nanyang Technological University** — **Singapore**
  Undergraduate Research Intern — *Feb 2013–Jun 2013*
  - Developed drivers and libraries for uCOS-III on TI-Evalbot

- **Qualcomm India Pvt Ltd** — **Bangalore, India**
  Interim Engineering Intern — *May 2012–Jul 2012*
  - Designed and prototyped DSDA system using Qualcomm chipsets

Publications

Books

1. Data Orchestration in Deep Learning Accelerators
   Tushar Krishna, Hyoukjun Kwon, **Ananda Samajdar**, Michael Pellauer, and Angshuman Parashar
   Morgan & Claypool Publishers

Preprints

1. *AIRCHITECT: Learning Custom Architecture Design and Mapping Space*
   Ananda Samajdar, Jan Moritz Joseph, Matthew Denton and Tushar Krishna
   arXiv preprint arXiv:2108.08295 - Aug 2021

2. *SCALE-Sim: Systolic cnn accelerator simulator*
   Ananda Samajdar, Yuhao Zhu, Paul Whatmough, Matthew Mattina, and Tushar Krishna
   arXiv preprint arXiv:1811.02883 - Oct 2018

Conference Proceedings

1. *Self Adaptive Reconfigurable Arrays (SARA): Learning Flexible GEMM Accelerator Configuration and Mapping-space using ML*
   Ananda Samajdar, Eric Qin, Michael Pellauer and Tushar Krishna
   Proc. of the 59th Annual Design Automation Conference, Jul 2022 **(DAC-2022)** *(To appear)*

2. *RASA: Efficient Register-Aware Systolic Array Matrix Engine for CPU*
   Geonhwa Jeong, Eric Qin, **Ananda Samajdar**, Christopher J. Hughes, Sreenivas Subramoney, Hyesoon Kim, Tushar Krishna
   Proc. of the 58th Annual Design Automation Conference, Dec 2021 **(DAC-2021)**

3. *Architecture, Dataflow and Physical Design Implications of 3D-ICs for DNN-Accelerators*
   Jan Moritz Joseph, **Ananda Samajdar**, Lingjun Zhu, Rainer Leupers, Sung Kyu Lim, Thilo Pionteck, Tushar Krishna
   22nd International Symposium on Quality Electronic Design **(ISQED-2021)**

4. *A Systematic Methodology for Characterizing Scalabitlity of DNN Accelerators using SCALE-Sim*
   Ananda Samajdar, Jan Moritz Joseph, Yuhao Zhu, Paul Whatmough, Matthew Mattina and Tushar Krishna
   Proc. of the 2020 Intl. Symposium on Performance Analysis of Systems and Software, April 2020 **(ISPASS-2020)**

5. *CLAN: Exploring Continuous Learning on Commodity Edge Devices using Asynchronous Distributed Neuroevolution*
   Parth Mannan, **Ananda Samajdar** and Tushar Krishna
   Proc. of the 2020 Intl. Symposium on Performance Analysis of Systems and Software, April 2020 **(ISPASS-2020)**

6. *SIGMA: A Sparse and Irregular GEMM Accelerator with Flexible DNN Training*
   Eric Qin, **Ananda Samajdar**, Hyoukjun Kwon, Vineet Nadella, Sudarshan Srinivasan, Dipankar Das, Bharat Kaul and Tushar Krishna
   Proc. of the 26th Intl. Symposium on High Performance Computer Architecture, Feb 2020 **(HPCA-2020)** (**Best paper award**)

7. *Scaling the Cascades: Interconnect-aware FPGA implementation of Machine Learning problems*
   Ananda Samajdar, Tushar Garg, Tushar Krishna and Nachiket Kapre
   Proc. of the 29th Intl. Conf. on Field Programmable Logic and Applications, Aug 2019 **(FPL-2019)**

8. *GeneSys: Enabling Continuous Learning through Neural Network Evolution in Hardware*
   Ananda Samajdar, Parth Mannan, Kartikay Garg and Tushar Krishna
   Proc. of the 51st IEEE/ACM Intl. Symp. on Microarchitecture, Oct 2018 **(MICRO-2018)**

9. *Euphrates: Algorithm-SoC Co-Design for Low-Power Mobile Continuous Vision*
   Yuhao Zhu, **Ananda Samajdar**, Matthew Mattina and Paul Whatmough
   Proc. of the ACM/IEEE 45th International Symposium on Computer Architecture **(ISCA-2018)**
   (Honourable Mention, IEEE MICRO Top Picks-2019)

10. *MAERI: Enabling Flexible Dataflow Mapping over DNN Accelerators via Reconfigurable Interconnects*
    Hyoukjun Kwon, **Ananda Samajdar** and Tushar Krishna
    Proc. of the 23rd ACM Int. Conf. on Architectural Support for Programming Languages and Operating Systems **(ASPLOS-2018)**
    (Honourable Mention, IEEE MICRO Top Picks-2019)

11. *Rethinking NoCs for Spatial Neural Network Accelerators*
    Hyoukjun Kwon, **Ananda Samajdar** and Tushar Krishna
    Proc. of the 11th IEEE/ACM International Symposium on Networks-on-Chip **(NOCS-2017)**

Journal Articles

1. *A Communication-driven Approach for Designing Flexible DNN Accelerators*
   Hyoukjun Kwon, **Ananda Samajdar** and Tushar Krishna
   Special Issue of **IEEE Micro** on Hardware Acceleration (Nov/Dec 2018)

2. *Algorithm-SoC Co-Design for Energy-Efficient Continuous Vision*
   Yuhao Zhu, **Ananda Samajdar**, Matthew Mattina, and Paul Whatmough
   (Honourable mention) Special issue of **IEEE Micro on Top-picks of computer architecture conferences** (May/Jun 2019)

3. *MAERI: A communication-driven approach to design a flexible and high-performance deep learning accelerator*
   Hyoukjun Kwon, **Ananda Samajdar** and Tushar Krishna
   (Honourable mention) Special issue of **IEEE Micro on Top-picks of computer architecture conferences** (May/Jun 2019)

Non-archived Articles

1. ACCELNET: *Learning Accelerator Design-Space*
   Ananda Samajdar, Jan Moritz Joseph and Tushar Krishna
   2021 Workshop on ML for Computer Architecture and Systems **(MLArchSys-2021)**

2. *Enabling Continuous Learning through Neural Network Evolution in Hardware*
   Ananda Samajdar, Kartikay Garg and Tushar Krishna
   3rd Workshop on Cognitive Architectures **(CogArch-2018)**

3. *Algorithm-SoC Co-Design for Energy-Efficient Mobile Continuous Vision*
   Yuhao Zhu, **Ananda Samajdar**, Matthew Mattina and Paul Whatmough
   3rd Workshop on Cognitive Architectures **(CogArch-2018)**

4. *MAERI: Enabling Flexible Dataflow Mapping over DNN Accelerators via Programmable Interconnects*
   Hyoukjun Kwon, **Ananda Samajdar** and Tushar Krishna
   Inaugral SysML Conference **(SysML-2018)**

Awards and Recognition

- **Invitation to present at DAC 2022 PhD Forum**
  Talk: Methodology and Analysis for Efficient Custom Architecture Design Using Machine Learning — *Jul 2022*
- **Best Paper Award at HPCA 2020**
  Talk: SIGMA: A Sparse and Irregular GEMM Accelerator with Flexible DNN Training — *Feb 2020*
- **Silver Medal at ACM student research competition at ASPLOS 2019**
  Talk: AIrchitect: Expert AI for accelerator design — *Apr 2019*

Talks

- **ACCELNET: Learning Accelerator Design-Space**
  Workshop talk at MLArchSys (at ISCA-2021), Virtual event — *Jun 2021*
- **A Systematic Methodology for Characterizing Scalability of DNN accelerators using SCALE-Sim**
  Conference talk at ISPASS-2020, Virtual event — *August 2020*
- **AIrchitect: Expert AI for accelerator design**
  ***Finalist** at the ACM Student Research Competition, Providence, RI, USA* — *April 2019*

- **GeneSys: Enabling continuous learning through neural network evolution on hardware**
  Conference talk at MICRO-2018, Fukuoka, Japan *October 2018*
- **GeneSys: Evolving Neural Networks in Hardware**
  ***Finalist** at the ACM Student Research Competition, Williamsburg,VA* *March 2018*
- **Enabling Continuous Learning through Neural Network Evolution in Hardware**
  Cogarch-2018 (Co-located with ASPLOS-2018), Williamsburg,VA *March 2018*
- **[Demo] SCALE-Sim: Systolic CNN Accelerator**
  Cogarch-2018 (Co-located with ASPLOS-2018), Williamsburg,VA *March 2018*

Artifacts

SCALE-Sim: Systolic CNN Accelerator Simulator https://github.com/ARM-software/SCALE-Sim

Technical skills

- **Programming Languages:** C, C++, Python, Matlab
- **HDLs:** Verilog, VHDL